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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,538	11/14/2003	Roberto Bez	2110-62-3	7956

7590 08/03/2006

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EXAMINER	
SMITH, BRADLEY	
ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 08/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,538	BEZ ET AL.	
	Examiner	Art Unit	
	Bradley K. Smith	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-23 and 26-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-23 and 26-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search notes*.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 19-23 and 26-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Mori (US Patent 6,989,303). Mori disclose a semiconductor body having a substrate a pair of insulation structures disposed in the substrate, delimiting an active area of the substrate, and each having respective portions projecting from said substrate, the projecting portions defining a recess over a portion of the active area and over a portion of at least one of the insulation structures; and a memory cell having body region disposed in the portion of the active area, a floating gate (22) disposed in the recess over the body region and over the portion of the at least one insulation structure, and a control gate (24) disposed over the floating gate (see figure 30 in the high and low voltage circuits). With regards to claim 20, Mori disclose said projecting portions define the recesses over respective portions of both of the insulation structures and said floating gate is disposed over the respective portions of both the insulating structures (see figure 30). With regards to claim 21 and 31, Mori disclose does the floating gate does not extend above the projecting portions of the insulating structures

(see figure 30).. With regards to claim 22 , Mori disclose does the floating gate does not extend beyond the projecting portions. With regards to claim 23, Mori disclose does the floating gate has a surface facing the control gate and the surface is planar (see figure 30).. With regards to claim 26, Mori disclose a substrate having an active region, first and second insulators disposed adjacent to the active region and defining a recess over a portion of the active region ; a body region of a memory cell disposed in the active region, and a floating gate of the memory cell disposed in the recess but not extending beyond the recess in a dimension parallel to a surface of the active region (see figure 30). With regards to claim 27, Mori disclose the first and second insulators first and second projections. With regards to claim 28 , Mori disclose first and second trenches disposed in the substrate', and wherein the first and second insulators are respectively disposed in the first and second trenches. With regards to claims 29 and 32, Mori disclose wherein the first and second insulators define the recesses over portions of the first and second insulators. With regards to claim 30, Mori disclose a gate insulator between the floating gate and the active region. With regards to claim 33, Mori disclose a gate insulator disposed on the floating gate ; and a control gate disposed on the gate insulator and overlapping the floating gate. With regards to claim 34, Mori disclose a first isolation region disposed in the substrate and defining a recess that is bounded by the isolation region on at least two sides and a first conductor disposed in the recess (see figure 30). With regards to claim 35, Mori disclose the insulator has projections that define the recess (see figure 30). With regards to claim 36, Mori disclose a trench in the substrate and the first insulation layer is in the trench. With regards to claims 37 the

examiner takes official notice that conductive regions inherently have resistivity and could be considered a resistor. With regards to claim 38, the examiner takes official notice that any conducive surface could be used a plate capacitor. With regards to claim 39 Mori disclose a second insulation layer over the first conductor and a second conductor over the second insulation layer.

Response to Arguments

Applicant's arguments with respect to claims 19-23 and 26-39 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

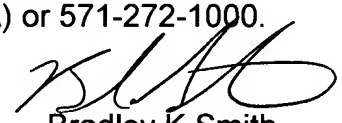
Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bradley K. Smith whose telephone number is 571-272-1884. The examiner can normally be reached on 10-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Bradley K Smith
Primary Examiner
Art Unit 2891